Please type a sign(+) inside this box → ⊞

PTO/SB/05 (2/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR § 1 53(b))

Attorney Docket No.	*15-4-833.00*
First Inventor or Application Identifier	*Alex Chalfin et al*
Title	*Synchronization of Hardware Simulation Processes*
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [Total Pages 22]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 9]

4. ☒ Oath or Declaration [Total Pages 9]

a. ☒ Newly executed (original or copy)

b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***

i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*

a. ☐ Computer Readable Copy

b. ☐ Paper Copy (identical to computer copy)

c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8 ☒ Assignment Papers (cover sheet & document(s))

9. ☐ 37 CFR 3 73(b) Statement (when there is an assignee) ☒ Power of Attorney

10 ☐ English Translation Document *(if applicable)*

11 ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations

12 ☐ Preliminary Amendment

13 ☒ Return Receipt Postcards (MPEP 503) *(Should be specifically itemized)*

14. ☐ *Small Entity Statement(s) *(PTO/SB/09-12)* ☐ Statement filed in prior application, Status still proper and desired

15 ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Other: 37 C F R § 1 136(a)(3) Authorization

☐ Other.

**NOTE FOR ITEMS 1 & 14 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R § 1 27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C F R §1 28)*

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment*

☐ Continuation ☐ Divisional ☐ Continuation-in-Part (CIP) of prior application No: ____/_____

Prior application information: *Examiner* _____ *Group/Art Unit:* _____

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* ☒ *Correspondence address below*

NAME	STERNE, KESSLER, GOLDSTEIN & FOX P L L C				
	Attorneys at Law				
ADDRESS	Suite 600, 1100 New York Avenue, N.W.				
CITY	Washington	*STATE*	DC	*ZIP CODE*	20005-3934
COUNTRY	USA	*TELEPHONE*	(202) 371-2600	*FAX*	(202) 371-2540

NAME (Print/Type)	Michael V. Messinger	*Registration No. (Attorney/Agent)*	37,575
SIGNATURE		*Date* 12/14/99	

Burden Hour Statement this form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

SKGF Rev 6/3/98 mac

1452.2900000trans

12/14/99 JC674 U.S. PTO

12/14/99 JC675 U.S. PTO 09/459995

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
ATTORNEYS AT LAW
1100 NEW YORK AVENUE, N.W., SUITE 600
WASHINGTON, D.C. 20005-3934

(202) 371-2600
FACSIMILE (202) 371-2540, (202) 371-6566

ROBERT GREENE STERNE
EDWARD J. KESSLER
JORGE A. GOLDSTEIN
SAMUEL L. FOX
DAVID K.S. CORNWELL
ROBERT W. ESMOND
TRACY-GENE G. DURKIN
MICHELE A. CIMBALA
MICHAEL B. RAY
ROBERT E. SOKOHL

ERIC K. STEFFE
MICHAEL Q. LEE
STEVEN R. LUDWIG
JOHN M. COVERT*
LINDA E. ALCORN
RAZ E. FLESHNER
ROBERT C. MILLONIG
MICHAEL V. MESSINGER
JUDITH U. KIM
TIMOTHY J. SHEA, JR.

DONALD R. MCPHAIL
PATRICK E. GARRETT
STEPHEN G. WHITESIDE
JEFFREY T. HELVEY*
HEIDI L. KRAUS
JEFFREY R. KURIN
RAYMOND MILLIEN
PATRICK D. O'BRIEN
LAWRENCE B. BUGAISKY
CRYSTAL D. SAYLES*

EDWARD W. YEE
ALBERT L. FERRO*
DONALD R. BANOWIT*
PETER A. JACKMAN
MOLLY A. MCCALL
TERESA U. MEDLER
JEFFREY S. WEAVER
KRISTIN K. VIDOVICH
ANDREW S. ROBERTS*
KENDRICK P. PATTERSON*

DONALD J. FEATHERSTONE**
KAREN R. MARKOWICZ**
GRANT E. REED**
SUZANNE E. ZISKA**
BRIAN J. DEL BUONO**
VINCENT L. CAPUANO**
ANDREA J. KAMAGE**
NANCY J. DEGEN**

ROBERT H. BENSON*
OF COUNSEL

*BAR OTHER THAN D.C.
**REGISTERED PATENT AGENTS

December 14, 1999

WRITER'S DIRECT NUMBER:
(202) 371-2667
INTERNET ADDRESS:
MIKEM@SKGF.COM

Assistant Commissioner for Patents
Washington, D.C. 20231

Box Patent Application

Re: U.S. Non-Provisional Utility Patent Application under 37 C.F.R. § 1.53(b)
Appl. No. (To be Assigned); Filed: Herewith
For: **Synchronization of Hardware Simulation Processes**
Inventors: Alex Chalfin et al.
Our Ref: 15-4-833.00

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. U.S. Utility Patent Application entitled:

Synchronization of Hardware Simulation Processes

and naming as inventors:

Alex Chalfin
Jeffrey Daudel
Mark Grossman
Shrijeet Mukherjee
Peter Ostrin
Jarrett Redd

the application comprising:

a. A specification containing:

(i) 16 pages of description prior to the claims;

(ii) 5 pages of claims (15 claims);

(iii) a one (1) page abstract;

b. 9 sheets of drawings: (Figures 1-9);

2. USPTO Utility Patent Application Transmittal Form PTO/SB/05;

3. Fee Transmittal Form PTO/SB/17 (in duplicate);

4. Originally executed Combined Declarations and Powers of Attorney;

5. Recordation Form Cover Sheet;

6. Executed Assignments to Silicon Graphics, Inc., recordation of which is hereby respectfully requested;

7. 37 C.F.R. § 1.136(a)(3) Authorization to Treat a Reply As Incorporating An Extension of Time (in duplicate);

8. Our Check No. 26184 in the amount of $956.00 to cover:
$760.00 Filing Fees
$40.00 Recordation Fees; and
$156.00 Excess Claim Fees

9. Three (3) return postcards.

It is respectfully requested that, of the three attached postcards, two be stamped with the filing date of these documents and returned to our courier, and the other prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. A duplicate copy of this letter is enclosed.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Michael V. Messinger
Attorney for Applicants
Registration No. 37,575

Enclosures
MVM:EWY nh
P \USERS\NHARRIS\egroup\EWY\1452\1452.2900000skgf

Synchronization of Hardware Simulation Processes

Inventors: Alex Chalfin
Jeffrey Daudel
Mark Grossman
Shrijeet Mukherjee
Peter Ostrin
Jarrett Redd

Background of the Invention

Field of the Invention

The present invention pertains to electronic system design, and more particularly to the simulation of digital circuitry.

Related Art

The process of designing and testing digital circuitry typically includes software simulation of the circuitry. Simulation takes place prior to development of a physical prototype, and allows economical testing of the logic of a circuit. Test vectors serve as inputs to the simulated circuitry, and the outputs are analyzed as a way of verifying the accuracy of the design.

A problem arises when a large amount of circuitry needs to be simulated. Simulation of a large circuit requires a large executable image, which can exceed the memory capacity of a simulation environment. Simulation of a system of circuits, such as a system of interoperating chips that perform in parallel, leads to the same problem. Current simulation methods deal with the image size problem by simulating a subset of the circuitry in any given test. Simulation of a subset of the circuitry creates an executable image having a more manageable size. By simulating a system portion by portion, all components of the system can be

tested. This creates some confidence in the accuracy of the logic of the overall system, but the value of such testing is limited. The system is never tested as a single entity, so that some doubt will remain as to the ability of the overall system to function as intended. As well as being incomplete, such testing is slow and costly. A simulation must be developed and executed for each of several subsets of the logic. Moreover, the identification of the appropriate subsets to be simulated can be difficult and time consuming.

In addition, the actual simulation of a system of components can be time consuming. Such a simulation typically proceeds sequentially, that is, step by step. At each step, a determination must be made as to which component(s) has (have) work to be done. The operation of the components must then be simulated, one component at a time. If the simulation of each component is viewed as a computational thread, then the simulation of a system of components, using current simulation methods, requires sequential execution of multiple threads. This is equivalent to the creation of a single large computational thread. While there are compilers that can parallelize simulations across multiple processors, their ability to perform load balancing and handle the different clocking requirements of multiple components is limited.

Hence, there is a need for a way to simulate a system of digital components, where the simulation is both efficient and logically comprehensive.

Summary of the Invention

The invention described herein is a system, method, and computer program product for simulating a system of hardware components. Each component simulated is described in a hardware definition language such as VERILOG or another high-level programming language sufficient to describe a hardware device. Each component is represented as a simulated device under test (DUT) that is incorporated into a simulation module. Each simulation module

can execute as an independent thread in parallel with all other simulation modules. The invention synchronizes the simulation modules by issuing clock credit to each simulation module. Each simulation module can only operate when clock credit is available, and can only operate for some number of clock cycles corresponding to the value of the clock credit. Operation is said to consume the clock credit. After a simulation module has consumed its clock credit, its DUT halts. Once every simulation module has consumed its clock credit and halted, another clock credit can be issued. This allows checkpointing of the operation of each DUT and simulates parallelism of the DUTs using executable images of manageable size.

A given DUT can include two or more subsets of logic that each require a clock signal having a different rate. Such subsets of the logic of a DUT are referred to as clock domains. The appropriate clock signals are generated by a test bench component of the simulation module. The test bench creates a master clock signal for the DUT. The test bench then divides this clock signal to produce clock signals applied to the clock domains of the DUT. The test bench can be created through automated means. Given a system specification that defines the inputs (including clocks) and outputs of a DUT, a test bench specific to the DUT can be created.

Features and Advantages

The invention described herein can provide clock signals of different rates to different clock domains of an individual DUT during simulation. The invention has the additional feature of being able to create a test bench that manages inputs and outputs specifically for a particular DUT during simulation. The invention has the additional feature of being able to simulate a system of DUTs while maintaining synchronization of the DUTs.

The invention has the advantage of simulating a complete system of DUTs without creating a single, excessively large executable image. The invention has the further advantage of simulating a system of DUTs in a relatively fast, efficient manner. In addition, the invention permits the simulation of an arbitrarily large number of DUTs in parallel.

Brief Description of the Figures

The foregoing and other features and advantages of the invention will be apparent from the following, more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings.

FIG. 1 is a block diagram generally illustrating the structure of an embodiment of the invention.

FIG. 2 illustrates the issuance of clock credit, according to an embodiment of the invention.

FIG. 3 illustrates the logical structure of a simulation module, according to an embodiment of the invention.

FIG. 4 is a flowchart illustrating the process of synchronizing simulation modules, according to an embodiment of the invention.

FIG. 5 is a flowchart illustrating the creation of clock signals for clock domains within a DUT, according to an embodiment of the invention.

FIG. 6 illustrates the provision of clock signals of different rates to different clock domains, according to an embodiment of the invention.

FIG. 7 illustrates generally the process of creating a test bench, according to an embodiment of the invention.

FIG. 8 is a flowchart illustrating in greater detail the process of creating a test bench, according to an embodiment of the invention.

FIG. 9 illustrates an example computing environment of the invention.

Detailed Description of the Preferred Embodiments

A preferred embodiment of the present invention is now described with reference to the figures where like reference numbers indicate identical or functionally similar elements. Also in the figures, the left most digit of each reference number corresponds to the figure in which the reference number is first used. While specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the relevant art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the invention. It will be apparent to a person skilled in the relevant art that this invention can also be employed in a variety of other devices and applications.

Contents

I. Terminology

The following section defines several terms that occur frequently throughout the application.

VERILOG is a language for simulation of digital circuitry and is an IEEE standard.

Device under test (DUT) refers to a block of VERILOG code (or other hardware simulation language) that, when executed, simulates a digital circuit or

a portion thereof for testing purposes. The device may be a chip, for example, or a subset of the logic on the chip.

Test bench refers to code that is ancillary to the DUT but operates in conjunction with the DUT. The test bench manages all inputs and outputs of the DUT, including clock signals, and can be written in VERILOG.

Programming language interface (PLI) is a body of code that interfaces the test bench with the rest of the system context that hosts the DUT during simulation. If the testbench is written in VERILOG and the surrounding system is written in C, the PLI serves as a VERILOG to C bridge.

Simulation module refers to the aggregate body of code that includes a DUT, the test bench for the DUT, and the associated PLI.

Clock credit is a token issued to a simulation module and having a numerical value, permitting the DUT to execute for some number of clock cycles associated with the value of the clock credit. Execution stops after the clock cycles have been used.

Clock domain refers to a portion of a DUT in which the circuitry is clocked at the same clock rate. A DUT may contain one or more distinct clock domains having different clock rates.

II. Overview

The invention described herein provides a system, method, and computer program product for the simulation of a system of hardware components, where the actual components operate in parallel. The invention provides a way to synchronize all of the components, thereby simulating operation of the complete system. Each component simulated is defined using the VERILOG programming language, or some other hardware simulation language. For each component, the VERILOG code is incorporated, along with additional support code, in a single simulation module. A clock arbitrator issues a clock credit to each simulation

module. This permits each simulation module to perform an amount of processing corresponding to the value of the clock credit. Once this amount of processing is completed, a given simulation module must halt. Once all the simulation modules have halted, then each simulation module has effectively consumed its clock credit. Further processing may not take place until the clock arbitrator issues an additional clock credit. This enables the clock arbitrator to maintain synchronization of each simulation module. This permits synchronized simulation of the complete system.

Each simulation module includes a test bench. A test bench consists of VERILOG code developed specifically for an associated component. If a given DUT contains two or more clock domains operating at distinct clock rates, the test bench serves to provide a clock signal with the appropriate clock rate to the appropriate domain of the DUT. Hence, the test bench serves to manage disparate clock rates on a given DUT. The testbench can also provide a means for interconnecting the interfaces of different DUTs. Note that a test bench can be created in an automated manner. This can be done by automated traversal of a machine-readable system design specification, identifying a DUT, and ascertaining the interfaces to the DUT.

III. System

The simulation environment is illustrated in general in FIG. 1. A clock arbitrator 105 is shown in relation to a plurality of simulation modules 110A through 110C. Clock arbitrator 105 is responsible for maintaining synchronization of the simulated system. Maintaining synchronization entails coordinating the processing of each DUT. As will be described in greater detail below, synchronization is maintained by issuance of clock credit. This is illustrated in greater detail in FIG. 2. Clock arbitrator 105 is shown issuing a clock credit 200 to each of simulation modules 110A through 110C. Upon

receipt of a clock credit 200, each simulation module allows its DUT to operate. Operation proceeds for a number of clock cycles corresponding to the value of clock credit 200. Once this is completed, clock credit 200 is considered to be consumed, and operation of the DUT halts. Once all the simulation modules have consumed their respective clock credits, then clock arbitrator can issue additional clock credit as necessary. Clock arbitrator 105 can be embodied in either software, firmware, or hardware. In an embodiment of the invention, clock arbitrator 105 is incorporated in a larger interface. This interface may include shared memory, and, in general, serves to represent the larger system within which the DUTs operate. In an embodiment of the invention, the shared memory serves to relay data between DUTs, so that data flows through the shared memory. Clock arbitrator 105 can identify synchronization points in the data flowing through the shared memory, that is, points in the data flow at which the DUTs must be synchronized. As a result, clock arbitrator 105 issues clock credit to the DUTs until a synchronization point is reached. Clock arbitrator 105 then stops issuing clock credit so that the DUTs halt at the synchronization point. Once the DUTs have halted, clock credit can be issued once again. This maintains synchronization of the DUTs.

Simulation modules are illustrated in greater detail in FIG. 3. A given simulation module includes a DUT 305. DUT 305 includes code that, when executed, simulates the operation of the physical circuit corresponding to DUT 305. The component represented by DUT 305 can be a chip, for example. DUT 305 can also be some subset of the logic contained on a chip. DUT 305 can be written in VERILOG or an alternative hardware simulation language. DUT 305 can also be written in a high-level simulation language, such as C, for faster operation. Like the circuitry that it simulates, DUT 305 requires a set of inputs and one or more clock signals. DUT 305 also produces one or more output signals. Note that some system components may not be undergoing testing, but

must nonetheless be simulated in order to fully simulate the dynamic behavior of the system. Such components can be modeled in a language such as C.

The clock signals, input signals, and output signals associated with DUT 305 are managed by a test bench 310. It is the responsibility of test bench 310 to provide input and clock signals to DUT 305 and to accept outputs produced by DUT 305. Because DUT 305 may include multiple clock domains, test bench 310 provides the necessary clock signal for each clock domain of DUT 305. Test bench 310 first creates a clock signal having a clock rate equivalent to the least common multiple of the clock rates required by the clock domains of DUT 305. This clock signal is referred to as the master clock signal. Clock signals for the various clock domains of DUT 305 are created by test bench 310. These clock rates are created by dividing the master clock rate. If, for example, a clock domain requires a 25 megahertz (MHz) clock signal while another clock domain requires a 20 MHz clock signal, a master clock signal having a frequency of 100 MHz will first be created. The 25 and 20 MHz signals are created by test bench 310 signal by dividing the 100 MHz signal by four and five, respectively. It is the responsibility of test bench 310 to create the needed clock signals by creating and manipulating the master clock signal.

Note that in some cases, the master clock signal will have a clock rate equal to the clock rate needed by one of the clock domains. Given two clock domains needing clock signals of 100 and 50 MHz, respectively, the master clock signal will have a clock rate of 100 MHz. In such a case, the master clock signal will be applied to the clock domain requiring that frequency.

Given the requirement that test bench 310 must manage all inputs and outputs of DUT 305, test bench 310 must be created specifically for DUT 305. Such a tailor-made test bench can be created by automated means. If, for example, a system of devices is specified in detail in a system database, test benches can be created by traversing the database, identifying the specific DUTs, and ascertaining the interfaces for each device. The interface information (that

is, the inputs, outputs, clock signals, and protocols for the device) can then be used to create a test bench specific for each component. The test bench can then be created in VERILOG, and compiled along with the VERILOG code representing the DUT, to create a single executable module.

A given simulation module also includes a programming language interface (PLI) 315. The function of the PLI 315 is to accept clock credit from a clock arbitrator and to enable the DUT 305 to operate for a number of clock cycles corresponding to the value of the received clock credit. Once DUT 305 has completed operation for that number of clock cycles, PLI 315 halts DUT 305. Operation of DUT 305 remains suspended until PLI 315 receives additional clock credit from the clock arbitrator. In an embodiment of the invention, a clock credit having a value of one corresponds to one clock cycle in DUT 305.

IV. Method

The method of the present invention includes the issuance of clock credit from a clock arbitrator to simulation modules. Each simulation module then executes for a number of clock cycles corresponding to the value of the received clock credit. Once a simulation module has completed execution of these clock cycles, its processing must halt pending receipt of additional clock credit. No further clock credit is issued until each simulation module has completed its allotted clock cycles. Within each simulation module, one or more clock signals are provided to the DUT. The test bench creates a master clock signal and creates slower clock signals by dividing the master clock signal appropriately.

The process of issuing clock credit and synchronizing simulation modules is illustrated in greater detail in FIG. 4, process 400. The process begins with a step 405. In a step 410, the clock arbitrator issues a clock credit to each simulation module. The DUT in each simulation module can then execute for a number of clock cycles corresponding to the value of the received clock credit.

In a step 415, the simulation modules begin execution in parallel. In a step 420, any active (i.e., executing) simulation module continues to execute. In a step 425, a determination is made as to whether the DUT of any simulation module has completed a number of clock cycles corresponding to the value of the received clock credit. If not, then the simulation modules continue execution in step 420. If the DUT of any simulation module has completed a number of clock cycles corresponding to the value of the received clock credit, then process 400 continues at a step 430. In step 430, execution of any DUT that has consumed its clock credit is halted. The corresponding simulation module is therefore no longer active. In a step 435, a determination is made as to whether all simulation modules have halted. If not, then process 400 continues at step 420. In step 420, any active simulation modules continue to execute. In this manner, the DUT of each simulation module executes only for a number of clock cycles corresponding to the value of the issued clock credit. Once all simulation modules have halted, then in a step 440, a determination is made as to whether additional clock credit must be issued to the system of simulation modules. If so, process 400 continues at step 410, and process 400 repeats. Otherwise, process 400 concludes at step 445.

When all of the simulation modules have completed an amount of processing corresponding to the value of the clock credit, then in step 435, index value i is equal to n, and processing continues in a step 445. In step 445, a determination is made as to whether additional clock credit is required. If so then the process returns to step 410 where additional clock credit is issued to each simulation module. Otherwise process 400 concludes at a step 450. In this manner, additional clock credit is only issued after each simulation module has completed an appropriate amount of processing. This permits a clock arbitrator to maintain synchronization of a plurality of simulation modules, corresponding to a respective plurality of DUTs.

Within any given simulation module, appropriate clock signals must be provided to the DUT. Moreover, different clock domains within a single DUT may require different clock rates. The provision of the requisite clock signals for a single DUT is described in greater detail in process 500 of FIG. 5. The process begins with a step 505. In a step 510, the PLI associated with a given DUT receives clock credit from the clock arbitrator. In a step 512, the test bench creates a master clock signal. The master clock signal has a clock rate equal to the least common multiple of the clock rates required by the clock domains of the DUT. In a step 515, the test bench divides the master clock signal as necessary to derive the clock signals required by the domains of the DUT. In a step 520, the test bench applies the resulting clock signals to the appropriate domains of the DUT. The process concludes with a step 525.

The operation of process 500 is illustrated graphically in FIG. 6. A clock credit 200 is shown being received by PLI 315 from clock arbitrator 105. Test bench 310 is made aware of the receipt of the clock credit 200. Given that test bench 310 is aware of the required clock rates for the various clock domains of DUT 305, test bench 310 provides the necessary clock signals to the clock domains of DUT 305. In particular, test bench 310 provides a clock signal 611 to clock domain 610, provides a clock signal 621 to clock domain 620, and provides a clock signal 631 to clock domain 630. As described above, the various clock rates are created by dividing the master clock rate so as to create the needed clock signals.

Note that a test bench specific to a DUT can be produced by automated means. This process is illustrated generally in FIG. 7. Assuming that all relevant system design information is encapsulated in a machine-readable form, the design information can be read to allow creation of a test bench specifically for each DUT of the system. The system design information can be encapsulated for example, in a design database 705. Design database 705 is read by a test bench development module 710. Test bench development module 710 steps through the

design information and identifies each DUT, and ascertains the signals that must go into and come out of each DUT. As a result, a test bench 310 specific to a DUT can be created, where test bench 310 is tailored to manage the inputs and outputs required by the DUT.

The process of creating a test bench is illustrated in greater detail as process 800 of FIG. 8. The process begins with a step 805. In a step 810, the test bench development module steps through the design information. In a step 815, the test bench development module identifies a DUT to be tested. In a step 820 the inputs and outputs for the DUT, including clock signals, are identified. In a step 830 the protocols of the inputs and outputs are determined for the DUT. The inputs, outputs, and protocols collectively constitute the interface of the DUT. In a step 840, the test bench is created based on the inputs, outputs, and protocols. The process concludes with a step 850.

V. Environment

The present invention may be implemented in a computer system or other processing system. An example of such a computer system 900 is shown in FIG. 9. The computer system 900 includes one or more processors, such as processor 904. The processor 904 is connected to a communication infrastructure 906, such as a bus or network). Various software implementations are described in terms of this exemplary computer system. After reading this description, it will become apparent to a person skilled in the relevant art how to implement the invention using other computer systems and/or computer architectures.

Computer system 900 also includes a main memory 908, preferably random access memory (RAM), and may also include a secondary memory 910. The secondary memory 910 may include, for example, a hard disk drive 912 and/or a removable storage drive 914, representing a floppy disk drive, a magnetic tape drive, an optical disk drive, etc. The removable storage drive 914

reads from and/or writes to a removable storage unit 918 in a well known manner. Removable storage unit 918, represents a floppy disk, magnetic tape, optical disk, or other storage medium which is read by and written to by removable storage drive 914. As will be appreciated, the removable storage unit 918 includes a computer usable storage medium having stored therein computer software and/or data.

In alternative implementations, secondary memory 910 may include other means for allowing computer programs or other instructions to be loaded into computer system 900. Such means may include, for example, a removable storage unit 922 and an interface 920. Examples of such means may include a program cartridge and cartridge interface (such as that found in video game devices), a removable memory chip (such as an EPROM, or PROM) and associated socket, and other removable storage units 922 and interfaces 920 which allow software and data to be transferred from the removable storage unit 922 to computer system 900.

Computer system 900 may also include a communications interface 924. Communications interface 924 allows software and data to be transferred between computer system 900 and external devices. Examples of communications interface 924 may include a modem, a network interface (such as an Ethernet card), a communications port, a PCMCIA slot and card, etc. Software and data transferred via communications interface 924 are in the form of signals 928 which may be electronic, electromagnetic, optical or other signals capable of being received by communications interface 924. These signals 928 are provided to communications interface 924 via a communications path (i.e., channel) 926. This channel 926 carries signals 928 and may be implemented using wire or cable, fiber optics, a phone line, a cellular phone link, an RF link and other communications channels.

In this document, the terms "computer program medium" and "computer usable medium" are used to generally refer to media such as removable storage

units 918 and 922, a hard disk installed in hard disk drive 912, and signals 928. These computer program products are means for providing software to computer system 900.

Computer programs (also called computer control logic) are stored in main memory 908 and/or secondary memory 910. Computer programs may also be received via communications interface 924. Such computer programs, when executed, enable the computer system 900 to implement the present invention as discussed herein. In particular, the computer programs, when executed, enable the processor 904 to implement the present invention. Accordingly, such computer programs represent controllers of the computer system 900. Where the invention is implemented using software, the software may be stored in a computer program product and loaded into computer system 900 using removable storage drive 914, hard drive 912 or communications interface 924. Simulation modules 110A through 110C are implemented in software and can therefore be loaded into computer system 900 through any of these means. Likewise, clock arbitrator 105 can also be implemented in software and can therefore be loaded into computer system 900 through any of these means.

A test bench development module can also be implemented in software on a system such as computer system 900 and can therefore be loaded into computer system 900 through any of these means. In such an embodiment, information from design database 705 can be read into computer system 900 through interface 924 or read from secondary memory 910. Test bench 310 can likewise be output through interface 924, or stored in secondary memory 910.

VI. Conclusion

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that

various changes in detail can be made therein without departing from the spirit and scope of the invention. Thus the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A method of synchronizing a plurality of simulation modules, comprising the steps of:

(a) issuing a clock credit to each simulation module;

(b) execution, by each simulation module, to an extent corresponding to the clock credit;

(c) for each simulation module, halting execution when the extent of execution corresponding to the clock credit has been completed; and

(d) when additional processing by at least one simulation module is necessary, issuing a further clock credit to each simulation module.

2. The method of claim 1, wherein step (a) comprises the step of issuing clock credit to each simulation module on the basis of synchronization points identified in data passing between the simulation modules.

3. The method of claim 1, further comprising, for one of the plurality of simulation modules, the steps of:

(e) creating a master clock signal;

(f) dividing the master clock signal to derive an additional clock signal; and

(g) applying the additional clock signal to one of the plurality of simulation modules,

wherein said steps (e) through (g) are performed after said step (a) and before said step (b).

4. The method of claim 3, wherein said steps (e), (f), and (g) are performed by a test bench component of the simulation module.

5. The method of claim 4, further comprising, before said step (e), the step of:

(h) creating a test bench component for the simulation module.

6. A method of creating a test bench component of a simulation module, the method comprising the steps of:

(a) reading specification information;

(b) identifying a device under test (DUT);

(c) determining the interface of the DUT; and

(d) generating the test bench component for the DUT, wherein the test bench component is capable of supporting testing of a plurality of clock domains of the DUT.

7. The method of claim 6, wherein said step (c) comprises the steps of:

(i) determining inputs and outputs of the DUT;

(ii) ascertaining attributes of the inputs and outputs; and

(iii) deriving a protocol of the inputs and outputs.

8. A system for synchronizing a plurality of simulation modules, comprising:

a clock arbitrator;

a programming language interface (PLI) for each simulation module, wherein said PLI receives a clock credit from said clock arbitrator and enables and halts simulation module execution on the basis of said clock credit; and

a test bench component for each simulation module, wherein said test bench component manages inputs and outputs to a device under test (DUT) within each simulation module.

9. The system of claim 8, wherein said clock arbitrator comprises a shared memory interface.

10. The system of claim 8, wherein said test bench component and said DUT are compiled together as a single binary executable module.

11. A computer program product comprising a computer usable medium having computer readable program code that enables a computer to synchronize a plurality of simulation modules, said computer readable program code comprising:

first computer readable program code logic for causing the computer to issue a clock credit to each simulation module;

second computer readable program code logic for causing the computer to execute each simulation module to an extent corresponding to the clock credit;

third computer readable program code logic for causing the computer to halt execution of a simulation module when the simulation module has completed execution to an extent corresponding to the clock credit; and

fourth computer readable program code logic for causing the computer to issue a further clock credit to each simulation module to perform additional execution by at least one simulation module.

12. The computer program product of claim 11, wherein said first computer readable program code logic comprises logic for causing the computer to issue clock credit to each simulation module on the basis of synchronization points identified in data passing between the simulation modules.

13. The computer program product of claim 11, further comprising:

fifth computer readable program code logic for causing the computer to create a master clock signal;

sixth computer readable program code logic for causing the computer to divide the master clock signal to derive an additional clock signal; and

seventh computer readable program code logic for causing the computer to apply the additional clock signal to one of the plurality of simulation modules.

14. A computer program product comprising a computer usable medium having computer readable program code that executes on a computer that creates a test bench component of a simulation module, said computer readable program code comprising:

first computer readable program code logic for causing the computer to read specification information;

second computer readable program code logic for causing the computer to identify a device under test (DUT);

third computer readable program code logic for causing the computer to determine the interface of the DUT; and

fourth computer readable program code logic for causing the computer to generate the test bench component for the DUT, wherein the test bench component is capable of supporting testing of a plurality of clock domains of the DUT.

15. The computer program product of claim 14, wherein said third computer readable program code logic comprises:

(i) computer readable program code logic for determining inputs and outputs of the module to be tested;

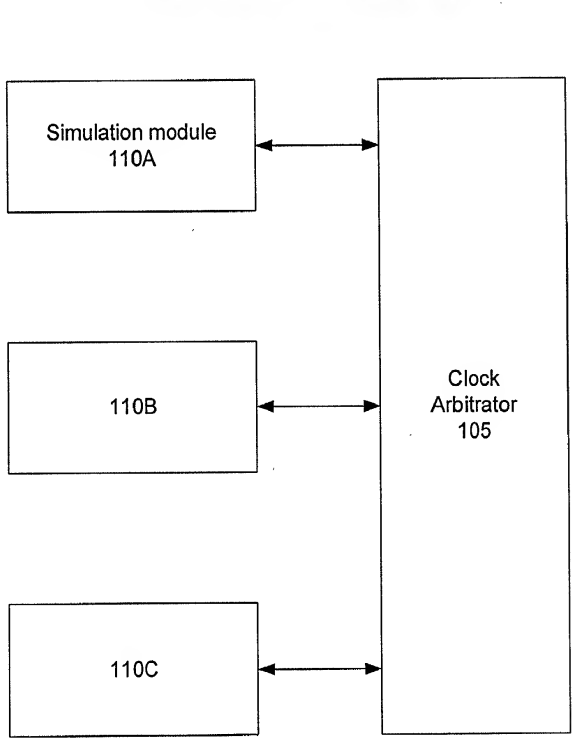
(ii) computer readable program code logic for ascertaining required attributes of the inputs and outputs; and

(iii) computer readable program code logic for deriving a protocol of the inputs and outputs.

Synchronization of Hardware Simulation Processes

Abstract

A system, method, and computer program product is presented for simulating a system of hardware components. Each component is simulated in a hardware definition language such as VERILOG. Each component is represented as a simulated device under test (DUT) that is incorporated into a simulation module. The invention synchronizes the simulation modules by issuing clock credit to each simulation module. Each simulation module can only operate when clock credit is available, and can only operate for some number of clock cycles corresponding to the value of the clock credit. Operation is said to consume the clock credit. After a simulation module has consumed its clock credit, its DUT halts. Once every simulation module has consumed its clock credit and halted, another clock credit can be issued. This allows checkpointing of the operation of each DUT and simulates parallelism of the DUTs using executable images of manageable size. A given DUT can include two or more subsets of logic that each require a clock signal having a different rate. Such subsets of the logic of a DUT are referred to as clock domains. The appropriate clock signals are created by a test bench component of the simulation module. The test bench creates a master clock signal for the DUT. The test bench then divides this clock signal to produce clock signals applied to the clock domains of the DUT. The test bench can be created through automated means by providing a system specification that defines the inputs (including clocks) and outputs of a DUT. This allows a test bench specific to the DUT to be created.



9907-28.vsd/1

FIG. 1

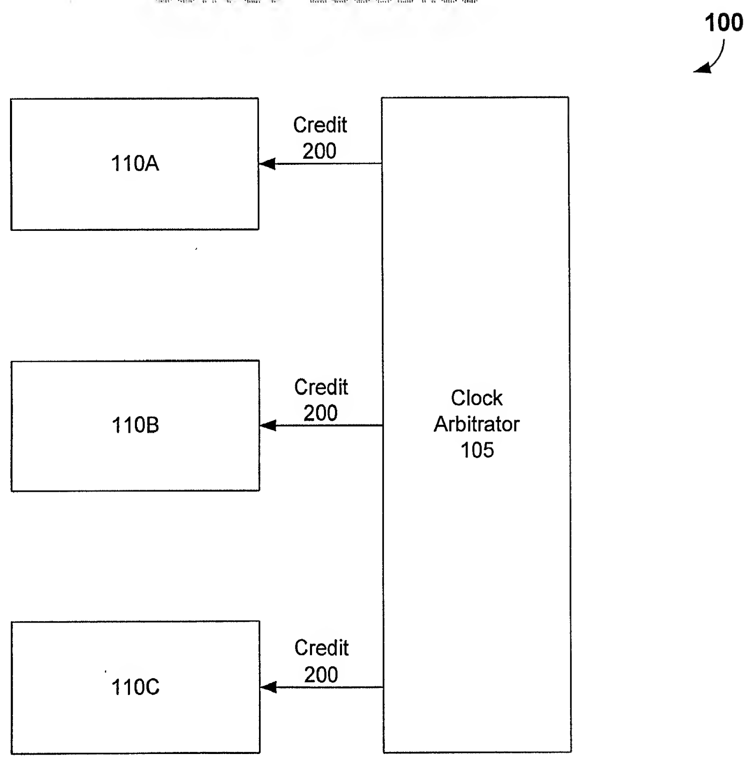


FIG. 2

9907-28.vsd/2

110A,

110B,

110C

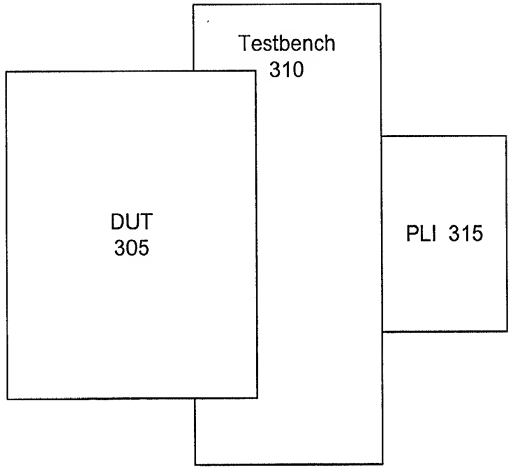


FIG. 3

9907-28.vsd/3

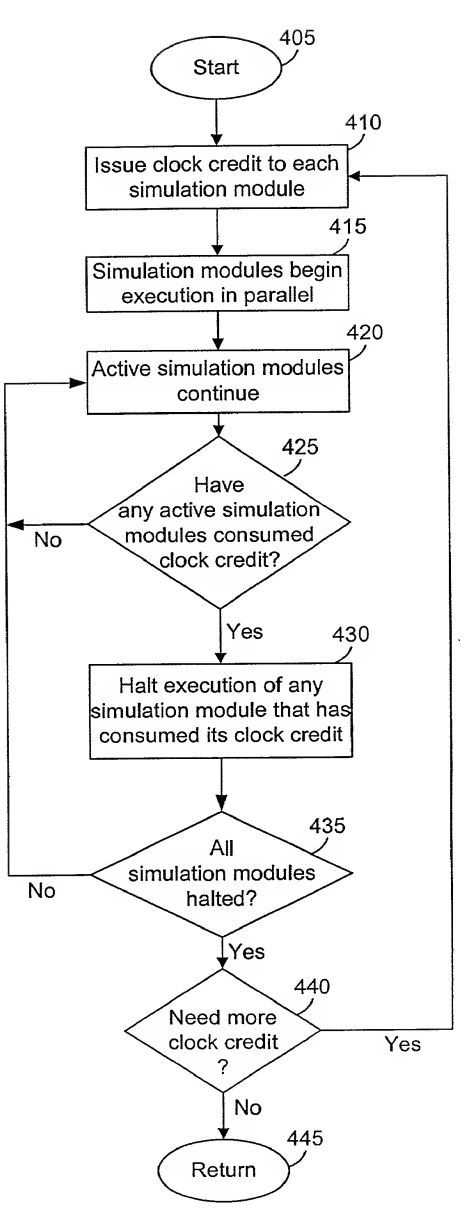

400
405
Start
410
Issue clock credit to each simulation module
415
Simulation modules begin execution in parallel
420
Active simulation modules continue
425
Have any active simulation modules consumed clock credit?
No
Yes
430
Halt execution of any simulation module that has consumed its clock credit
435
All simulation modules halted?
No
Yes
440
Need more clock credit ?
Yes
No
445
Return
9907-28.vsd/4

FIG. 4

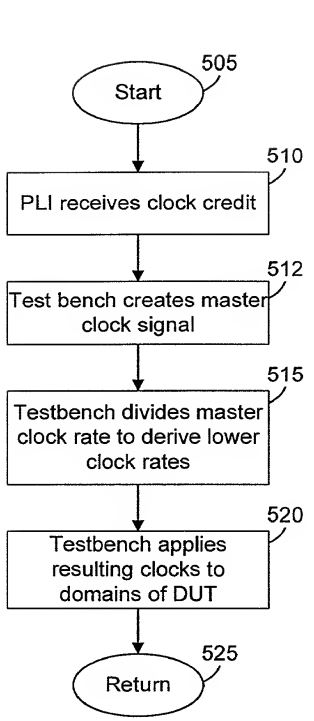


FIG. 5

9907-28.vsd/5

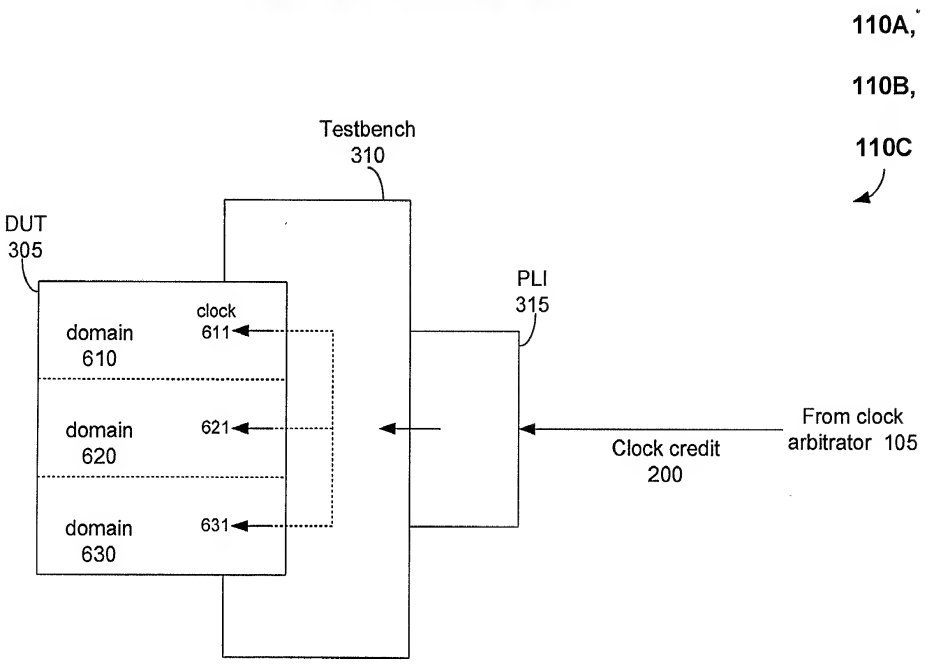


FIG. 6

9907-28.vsd/6

700

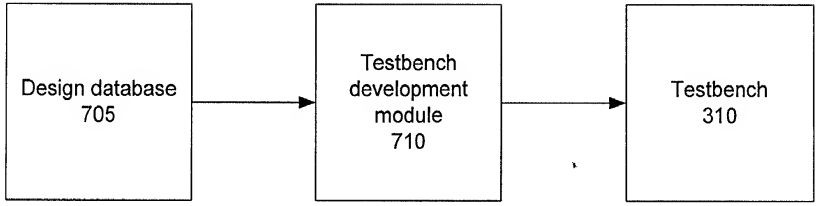
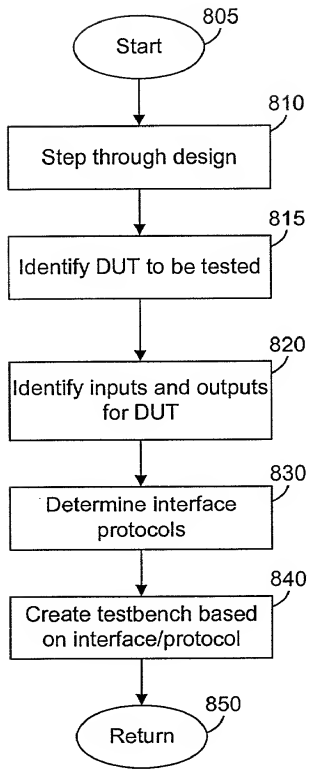


FIG. 7

9907-28.vsd/7



9907-28.vsd/8

FIG. 8

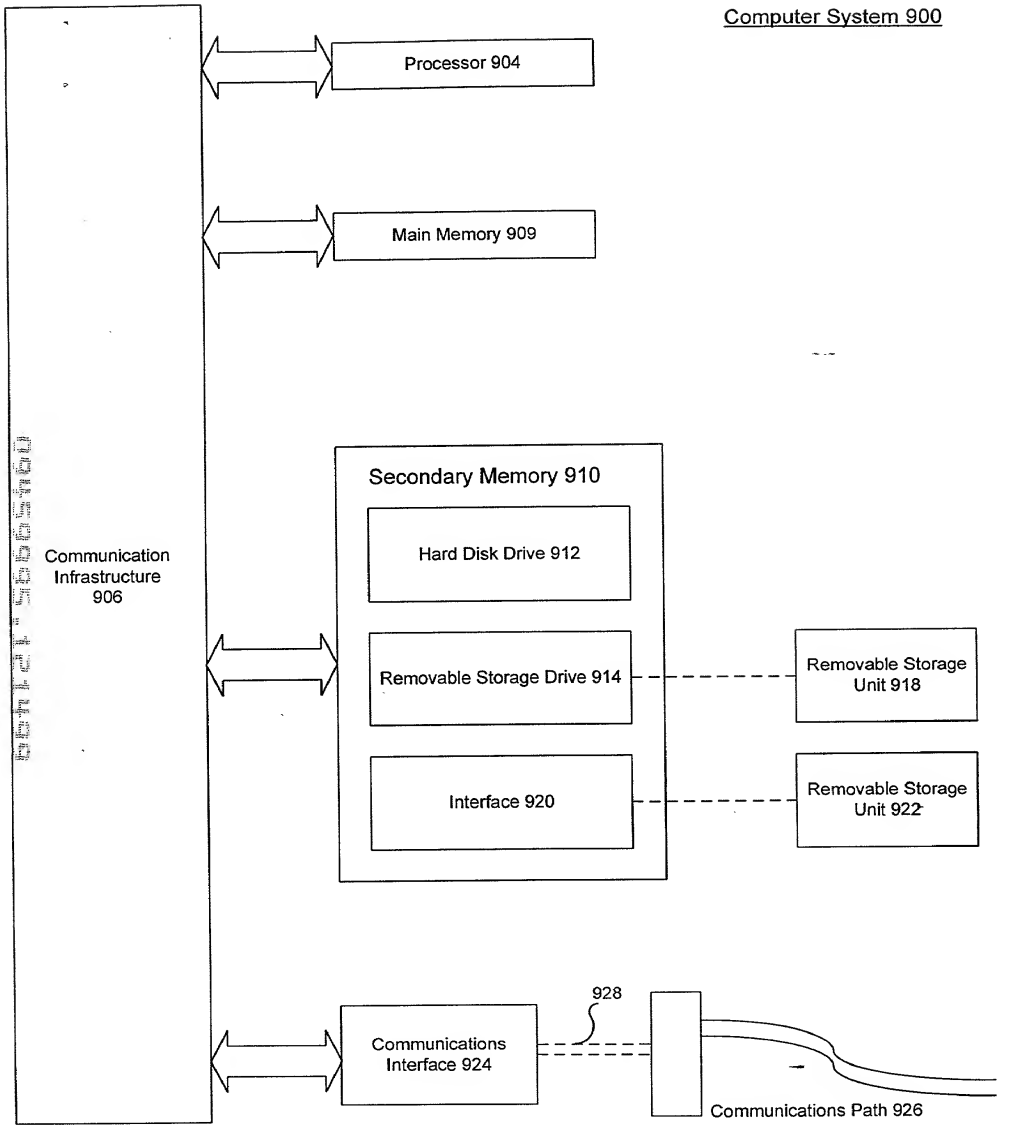


FIG. 9

9907-28.vsd/9

Combined Declaration and Power of Attorney for Patent Application

Docket Number: 15-4-833.00

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled Synchronization of Hardware Simulation Processes, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____;
as United States Application Number or PCT International Application Number_____; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____ (Application No.)	_____ (Filing Date)
_____ (Application No.)	_____ (Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)
_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Douglas J. Crisman, Reg. No. 39,951; John Brigden, Esq., Reg. No. 40,530;

Robert G. Sterne, Esq., Reg. No. 28,912; Edward J. Kessler, Esq., Reg. No. 25,688; Jorge A. Goldstein, Esq., Reg. No. 29,021; Samuel L. Fox, Esq., Reg. No. 30,353; David K.S. Cornwell, Esq., Reg. No. 31,944; Robert W. Esmond, Esq., Reg. No. 32,893; Tracy-Gene G. Durkin, Esq., Reg. No. 32,831; Michele A. Cimbala, Esq., Reg. No. 33,851; Michael B. Ray, Esq., Reg. No. 33,997; Robert E. Sokohl, Esq., Reg. No. 36,013; Eric K. Steffe, Esq., Reg.No. 36,688; Michael Q. Lee, Esq., Reg. No. 35,239; and Steven R. Ludwig, Reg. No. 36,203.

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor	Alex Chalfin
Signature of sole or first inventor	Date
Residence	600 Rainbow Drive #181 Mountain View, CA 94041
Citizenship	USA
Post Office Address	
Full name of second inventor	Jeffrey Daudel
Signature of second inventor	Date
Residence	1655 Pomeroy Avenue #9 Santa Clara, CA 95051
Citizenship	USA
Post Office Address	

Full name of third inventor	Mark Grossman
Signature of third inventor	Date
Residence	2063 Bryon St Palo Alto, CA 94301
Citizenship	USA
Post Office Address	

Full name of fourth inventor	Shrijeet Mukherjee
Signature of fourth inventor	Date
Residence	840 Alice Avenue #21 Mountain View, CA 94041
Citizenship	India
Post Office Address	

Full name of fifth inventor	Peter Ostrin
Signature of fifth inventor	Date
Residence	932 W. Olive Avenue Sunnyvale, CA 94086
Citizenship	South Africa
Post Office Address	

Full name of sixth inventor	Jarrett Redd
Signature of ~~fifth~~ sixth inventor	Nov 29, 1999 Date
Residence	10456 Porter Lane San Jose, CA 95127-2597
Citizenship	USA
Post Office Address	

P:\USERS\PDOMALLY\1452.2900000dec

(Supply similar information and signature for subsequent joint inventors, if any)

Combined Declaration and Power of Attorney for Patent Application

Docket Number: 15-4-833.00

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled Synchronization of Hardware Simulation Processes, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____;
as United States Application Number or PCT International Application Number_____; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____ (Application No.)	_____ (Filing Date)
_____ (Application No.)	_____ (Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)
_____ (Application No.)	_____ (Filing Date)	_____ (Status - patented, pending, abandoned)

Appl. No. (to be assigned)
Docket No. 15-4-833.00

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Douglas J. Crisman, Reg. No. 39,951; John Brigden, Esq., Reg. No. 40,530;

Robert G. Sterne, Esq., Reg. No. 28,912; Edward J. Kessler, Esq., Reg. No. 25,688; Jorge A. Goldstein, Esq., Reg. No. 29,021; Samuel L. Fox, Esq., Reg. No. 30,353; David K.S. Cornwell, Esq., Reg. No. 31,944; Robert W. Esmond, Esq., Reg. No. 32,893; Tracy-Gene G. Durkin, Esq., Reg. No. 32,831; Michele A. Cimbala, Esq., Reg. No. 33,851; Michael B. Ray, Esq., Reg. No. 33,997; Robert E. Sokohl, Esq., Reg. No. 36,013; Eric K. Steffe, Esq., Reg.No. 36,688; Michael Q. Lee, Esq., Reg. No. 35,239; and Steven R. Ludwig, Reg. No. 36,203.

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SCANNED

Full name of sole or first inventor	Alex Chalfin	
Signature of sole or first inventor		Date
Residence	600 Rainbow Drive #181 Mountain View, CA 94041	
Citizenship	USA	
Post Office Address		
Full name of second inventor	Jeffrey Daudel	
Signature of second inventor	Jeffrey Daudel	12/3/99 Date
Residence	1655 Pomeroy Avenue #9 Santa Clara, CA 95051	
Citizenship	USA	
Post Office Address	1655 Pomeroy Ave #9 Santa Clara, CA 95051-2847	

Full name of third inventor	Mark Grossman
Signature of third inventor	Date
Residence	2063 Bryon St. Palo Alto, CA 94301
Citizenship	USA
Post Office Address	

Full name of fourth inventor	Shrijeet Mukherjee
Signature of fourth inventor	Date
Residence	840 Alice Avenue #21 Mountain View, CA 94041
Citizenship	India
Post Office Address	

Full name of fifth inventor	Peter Ostrin
Signature of fifth inventor	Date
Residence	932 W. Olive Avenue Sunnyvale, CA 94086
Citizenship	South Africa
Post Office Address	

Full name of sixth inventor	Jarrett Redd
Signature of fifth inventor	Date
Residence	10456 Porter Lane San Jose, CA 95127-2597
Citizenship	USA
Post Office Address	

P:\USERS\PDOMALLY\1452 2900000dec

(Supply similar information and signature for subsequent joint inventors, if any)

Combined Declaration and Power of Attorney for Patent Application

Docket Number: 15-4-833.00

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled Synchronization of Hardware Simulation Processes, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____;
as United States Application Number or PCT International Application Number_____; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____	_____	_____	☐ Yes ☐ No
(Application No.)	(Country)	(Day/Month/Year Filed)	
_____	_____	_____	☐ Yes ☐ No
(Application No.)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____	_____
(Application No.)	(Filing Date)
_____	_____
(Application No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

_____	_____	_____
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)
_____	_____	_____
(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Douglas J. Crisman, Reg. No. 39,951; John Brigden, Esq., Reg. No. 40,530;

Robert G. Sterne, Esq., Reg. No. 28,912; Edward J. Kessler, Esq., Reg. No. 25,688; Jorge A. Goldstein, Esq., Reg. No. 29,021; Samuel L. Fox, Esq., Reg. No. 30,353; David K.S. Cornwell, Esq., Reg. No. 31,944; Robert W. Esmond, Esq., Reg. No. 32,893; Tracy-Gene G. Durkin, Esq., Reg. No. 32,831; Michele A. Cimbala, Esq., Reg. No. 33,851; Michael B. Ray, Esq., Reg. No. 33,997; Robert E. Sokohl, Esq., Reg. No. 36,013; Eric K. Steffe, Esq., Reg.No. 36,688; Michael Q. Lee, Esq., Reg. No. 35,239; and Steven R. Ludwig, Reg. No. 36,203.

Send Correspondence to:

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934

Direct Telephone Calls to:

(202) 371-2600

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor	Alex Chalfin
Signature of sole or first inventor	Date 11/29/99
Residence	600 Rainbow Drive #181 Mountain View, CA 94041
Citizenship	USA
Post Office Address	
Full name of second inventor	Jeffrey Daudel
Signature of second inventor	Date
Residence	1655 Pomeroy Avenue #9 Santa Clara, CA 95051
Citizenship	USA
Post Office Address	

Full name of third inventor	Mark Grossman
Signature of third inventor	29 NOV 99 Date
Residence	2063 Bryon St. Palo Alto, CA 94301
Citizenship	USA
Post Office Address	

Full name of fourth inventor	Shrijeet Mukherjee
Signature of fourth inventor	Date 11/28/1999
Residence	840 Alice Avenue #21 Mountain View, CA 94041
Citizenship	India
Post Office Address	

Full name of fifth inventor	Peter Ostrin
Signature of fifth inventor	Date 11/29/99
Residence	932 W. Olive Avenue Sunnyvale, CA 94086
Citizenship	South Africa
Post Office Address	

Full name of sixth inventor	Jarrett Redd
Signature of fifth inventor	Date
Residence	10456 Porter Lane San Jose, CA 95127-2597
Citizenship	USA
Post Office Address	

P:\USERS\PDOMALLY\1452 2900000doc

(Supply similar information and signature for subsequent joint inventors, if any)